Electronic Version
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Claims

[c1] 1.An ESD NMOSFET with a lower trigger voltage comprising:
a substrate having first, second and third wells formed in said substrate, and separated by shallow well isolation regions, said first and third wells connected along a bottom thereof with a conductive band region generally separating the bottom of said second well from said substrate;
a source and drain region in said second well forming an FET, said drain being connected to an I/O pad for protecting said pad against an ESD event; and
a path of substrate material extending through an opening in said conductive band region, to increase the substrate resistance in the path of the current which flows through said I/O pad to a substrate contact and drain during an ESD event.

[c2] 2.An ESD NMOSFET according to claim 1 wherein said substrate has a contact which is outside of said first, second and third wells.

[c3] 3.An ESD NMOSFET according to claim 1 wherein said first and third wells are N-wells and said conductive

band region comprises a semiconductor region which is N doped.

[c4] 4.An ESD NMOSFET according to claim 3 wherein said conductive band region is segmented forming said resistive path to said substrate.

[c5] 5.The ESD NMOSFET according to claim 1 wherein said FET has a gate connection and source connected to said substrate contact.

[c6] 6.The ESD NMOSFET according to claim 1 wherein said drain is connected through a matching impedance to said I/O pad to provide a signal from a circuit on said substrate to said I/O pad.

[c7] 7.A method for decreasing the trigger voltage of an ESD NMOSFET comprising:
locating said ESD NMOSFET in a well of a triple well CMOS structure, and connecting said ESD NFET to an I/O pad; and
providing a resistive path from said first well to a substrate contact located outside of said wells, whereby the trigger voltage of the said ESD NMOSFET is reduced due to said resistive path between said substrate contact and said I/O pad.

[c8] 8.The method according to claim 7 wherein said resistive

path is an opening in said well to form a connection between said NMOSFET and said substrate contact.

[c9] 9.The method according to claim 7 wherein said well is an P-well with an N-band of N doped semiconductor material which separates said N-well from said substrate, and which includes an opening forming said resistive path.

[c10] 10.The method according to claim 7 wherein said ESD NMOSFET further comprising connecting a gate connection and a source of said NMOSFET to said substrate contact. .

[c11] 11. The method according to claim 7 wherein a second and third well of said triple well structure are N-Wells, and one of said N-wells is connected to said substrate contact.

[c12] 12.The method according to claim 7 further comprising connecting a gate of said Nto said substrate contact.

[c13] 13.An ESD NMOSFET with a lower trigger voltage comprising:substrate having first, second and third wells formed in said substrate, said first well comprising a P-well separated from second and third N-Wells by shallow well isolation regions, said first well separated from said substrate along a bottom thereof with a conductive band

region;substrate contact outside of said first, second and third wells;

a source and drain region in said P Well forming an FET, said drain being connected to an 1/O pad for protecting said pad against an ESD event; and

a resistive path extending through an opening in said conductive band region to said substrate contact, said resistive path decreasing the trigger voltage for said FET.

[c14] 14.The ESD NMOSFET according to claim 13 wherein said FET source and gate are connected to substrate contact.

[c15] 15.The ESD NMOSFET according to claim 13 wherein said source is connected to said substrate contact.